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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,717	06/25/2001	Jerrell Hein	026-0006	8760

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EXAMINER

AHN, SAM K

ART UNIT PAPER NUMBER

2611

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

20

Office Action Summary	Application No.		Applicant(s)	
	09/888,717		HEIN ET AL.	
	Examiner		Art Unit	
	Sam K. Ahn		2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 and 9 is/are allowed.
- 6) ☒ Claim(s) 1-7, 10-19 and 22-25 is/are rejected.
- 7) ☒ Claim(s) 20 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see p.3, filed 09/05/06, with respect to the rejection(s) of claim(s) 1-7,11,15-17 and 24 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tamamura and in view of Harrison US 6,470,060 B1 and Suzuki et al. US 4,647,984 (Suzuki).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-7,11,15-17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura US 6,118,316 (cited previously) in view of Harrison US 6,470,060 B1 (cited previously) and Suzuki et al. US 4,647,984 (Suzuki).

Regarding claim 1, Tamamura teaches a clock recovery circuit (see Fig.4) comprising: a phase detector circuit (201-1) to generate a difference signal (201a-1) indicating a phase difference between an incoming data stream (1 1-1) and a delayed clock signal (201a-1); an oscillator circuit (203-1) responsive to a control signal (202a-1) derived from the difference signal (201a-1) to generate an output clock signal (output of 203-1) variable according to the control signal, and

a clock delay circuit (204-1) coupled to receive the output clock signal.

However, Tamamura does not teach the clock delay circuit receiving a delay control signal derived from the difference signal and provide as the delayed clock signal.

Stubbs teaches a clock delay circuit (108 in Fig.1 delaying clock signal 102) coupled to receive a delay control signal (132,134) derived from the difference signal (the difference between the E_CLOCK AND I_CLOCK, note col.4, lines 35-36, and produces the delay control signal accordingly).

Therefore, both Tamamura and Stubbs teach a clock delay circuit adjusting the delay, wherein the clock delay circuit is coupled to the phase detector circuit.

Tamamura teaches the clock delay circuit (204-1) delaying the signal according to a division ratio n of the divider (note col.14, lines 59-60), on the other hand, Stubbs teaches the clock delay circuit (108) delaying the signal according to the delay control signal (132,134), wherein Stubbs further suggests that through the delay control signal variable delay adjustments can be processed quickly and locks into the signal quickly in an integrated circuit (note col.4, lines 19-25). The integrated circuit of Tamamura can benefit from the incorporation of the teaching of Stubbs by providing the delay control signal for the purpose of quickly locking in to the signal. Hence, through the combination of Tamamura and Stubbs, one skilled in the art would recognize that the clock delay circuit (204-1) coupled to provide as the delayed clock signal (204a-1) the output clock signal (output of 203-1) delayed according to the delay control signal (132,134 of Stubbs).

However, Tamamura in view of Stubbs do not explicitly teach the variable delay line coupled to receive the output clock signal from the oscillator circuit.

Suzuki teaches a variable delay line (1 in Fig.1) coupled to receive output clock signal from the oscillator circuit (6 in Fig.1). Hence both Stubbs and Suzuki teach the variable delay line, wherein Suzuki further suggests that the VCO providing the output clock signal to the variable delay line properly drives the variable delay line by proper phase difference (note col.3, lines 43-56). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Suzuki in the teaching of Stubbs of coupling the variable delay line to the VCO of Suzuki for the purpose of properly driving the variable delay line by proper phase difference (note col.3, lines 43-56).

Regarding claim 2, Tamamura further teaches comprising a loop filter (202-1) coupled to receive the difference signal and supply a filtered output as the control signal.

Regarding claim 3, Tamamura further teaches wherein the control signal (202a-1) for the oscillator circuit (203-1) is used as the delay control signal (provided to 204-1).

Regarding claim 4, Tamamura in view of Stubbs and Suzuki teach all subject matter claimed, as applied to claim 1 or 15, as previously explained, teach generating the

delay control signal derived from the difference signal, however, do not explicitly teach a delay control filter circuit coupled to receive the difference signal. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement as such. Applicant has not disclosed that the delay control filter coupled to receive the difference signal provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with or without the delay control filter because Stubbs teaches fine and coarse adjustment control signal which quickly adjusts variable delay. One skilled in the art would further recognize that a filter can be implemented at any part of a system in order to eliminate any undesirable noise or error. Therefore, it would have been obvious to to one of ordinary skill in this art to modify the teaching of Tamamura in view of Stubbs to obtain the invention as specified in claim.

Regarding claim 5, as previously explained, teach the clock delay circuit, however, do not explicitly teach wherein the clock delay circuit is a voltage controlled delay circuit. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement as such. Voltage controlled delay circuit or voltage controlled oscillator circuit is well-known to one skilled in the art. Applicant has not disclosed that the clock delay circuit is a voltage controlled delay circuit or

voltage controlled oscillator circuit provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with providing control signals as taught by Stubbs in Fig.3 of providing a control signal (320 – 326) to control the delay because it provides delay control quickly, as taught by Stubbs. Therefore, it would have been obvious to one of ordinary skill in this art to modify the teaching of Tamamura in view of Stubbs to obtain the invention as specified in claim.

Regarding claim 6, Stubbs further teaches wherein the clock delay circuit comprises multiple stages (304,308...316).

Regarding claim 7, Stubbs further teaches wherein through the coarse and fine adjustments, the clock signal is adjusted (see Fig.3) and the delay cells (304-316) have a period less than one period of the output clock signal in order to accurately adjust the delay (note col.4, line 52 – col.5, line 12).

Regarding claim 11, the claim is rejected as applied to claim 5 with similar scope.

Regarding claim 12, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 15, the claim is rejected as applied to claim 1 with similar scope.

Regarding claim 16, the claim is rejected as applied to claim 3 with similar scope.

Regarding claim 24, the claim is rejected as applied to claim 1 with similar scope.

3. Claims 10,12,13,18,19,22,23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura et al. USP 6,118,316 (Tamamura, cited previously) in view of Stubbs US 6,959,062 B1 (cited previously) and Suzuki et al. US 4,647,984 (Suzuki) and in further view of Kaylani et al. USP 6,711,227 B1 (Kaylani, cited previously).

Regarding claim 10, Tamamura in view of Stubbs and Suzuki teach all subject matter claimed, as applied to claim 1. However, Tamamura in view of Stubbs and Suzuki do not teach a first in first out (FIFO) memory coupled to write data into the FIFO memory with the delayed clock signal and to read data out of the FIFO memory with the output clock signal, thereby retiming data to the output clock signal. Kaylani teaches a data recovery circuit in a FIFO memory (50 in Fig.5) coupled to write data into the FIFO memory with a clock signal (20) and to read data out of the FIFO memory with the output clock signal (16, output of a PLL having a phase detector), thereby retiming data to the output clock signal. And although Kaylani does not explicitly teach the clock signal is the delayed clock signal, it would have been obvious to one skilled in the art at the time of the invention to write to the FIFO memory using the delayed clock signal for the purpose of synchronizing the FIFO memory to the delayed clock signal, which has been adjusted, thus receive a more synchronous signal.

And further, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Kaylani of having the data recovery circuit comprising the FIFO memory in the system of Tamamura for the purpose

of recovering data with through the clock recovery in the case of receiving signals, such as Manchester coded signals wherein data and clock are combined into the signal, thus synchronize the system based on the received signal.

Regarding claim 12, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 13, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 18, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 22, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 23, the claim is rejected as applied to claim 10 with similar scope.

Regarding claim 25, the claim is rejected as applied to claim 10 with similar scope.

Regarding claims 19, Tamamura in view of Suzuki teach all subject matter claimed, as applied to claim 18, and further teaches wherein the clock delay circuit (7) is a voltage controlled delay circuit (see Fig.2 and note col.4, lines 34-42) and comprises multiple stages (by having plurality of inverters, 10), and wherein a delay period from one stage to a next stage in the clock delay circuit is less than one period of the output clock signal (note col.4, lines 39-42 wherein the total delay time is adjusted by controlling each of the inverters).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamamura

et al. USP 6,118,316 (Tamamura, cited previously) in view of Stubbs US 6,959,062 B1 (cited previously) and Suzuki et al. US 4,647,984 (Suzuki) and in further view of Bulzachelli (cited previously in the IDS).

Regarding claim 14, Tamamura in view of Stubbs and Suzuki teach all subject matter claimed, as applied to claim 1.

Tamamura further teaches a closed loop (2OA in Fig.4), however, do not explicitly teach having the closed loop response without an explicit zero. Bulzachelli also teaches a phase detector (see 102 and 202 in Figs. 1 and 2) having a closed loop response and further teaches the loop amplifier and filter having an integrator plus other circuitry and contains an explicit zero. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the teaching of Bulzachelli in the system of Tamamura having the integrator and other circuitry to provide an explicit zero for the purpose of providing a loop stability, as taught by Bulzachelli (note col.3, lines 20-32).

Allowable Subject Matter

5. Claims 8 and 9 are allowed.
6. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowable subject matter:
Present application discloses clock recovery circuit wherein the incoming signal is

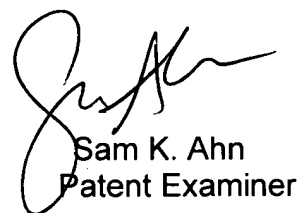
Art Unit: 2611

retimed to recover proper timing of the incoming signal. Prior art teaches or suggests in combination all the limitations claimed. However, prior art does not teach wherein the phase comparator is coupled to provide its output to serial registers with the configuration of the elements of having the first and last registers as illustrated in the seventh figure of receiving from the delay stages of the clock delay circuit and the phase comparator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Ahn whose telephone number is (571) 272-3044. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Sam K. Ahn
Patent Examiner

11/13/06